EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	124	forward adj body adj bias	US-PGPUB; USPAT; USOCR; EPO; JPO	OR	ON	2007/11/12 09:43
L2	74	tang-stephen-h$.in.	US-PGPUB; USPAT; USOCR; EPO; JPO	OR	ON	2007/11/12 09:43
L3	82	khellah-muhammad-m$.in.	US-PGPUB; USPAT; USOCR; EPO; JPO	OR	ON	2007/11/12 09:43
L4	117	somasekhar-dinesh.in.	US-PGPUB; USPAT; USOCR; EPO; JPO	OR	ON	2007/11/12 09:43
L5	256	de-vivek-k$.in.	US-PGPUB; USPAT; USOCR; EPO; JPO	OR	ON	2007/11/12 09:44
L6	69	tschanz-james-w$.in.	US-PGPUB; USPAT; USOCR; EPO; JPO	OR	ON	2007/11/12 09:44

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Time: 09:39:43

Inventor Name Search Result

Your Search was:

Last Name = TANG
First Name = STEPHEN

Application#	Patent#	Status	Date Filed	Title	Inventor Name
10748222	6903984	150	12/31/2003	FLOATING-BODY DRAM USING WRITE WORD LINE FOR INCREASED RETENTION TIME	TANG, STEPHEN
10987278	Not Issued	41	11/12/2004	Level shifter	TANG, STEPHEN
11066395	7031203	150	02/28/2005	FLOATING-BODY DRAM USING WRITE WORD LINE FOR INCREASED RETENTION TIME	TANG, STEPHEN
11111060	7199617	150	04/21/2005	LEVEL SHIFTER	TANG, STEPHEN
10014009	Not Issued	161	12/10/2001	BALANCING GATE-LEAKAGE CURRENT IN DIFFERENTIAL PAIR CIRCUITS	TANG, STEPHEN H.
10025047	6693332	150	12/19/2001	CURRENT REFERENCE APPARATUS	TANG, STEPHEN H.
10162929	6643199	150	06/04/2002	MEMORY WITH REDUCED SUB-THRESHOLD LEAKAGE CURRENT IN DYNAMIC BIT LINES OF READ PORTS	TANG, STEPHEN H.
10267951	6784722	150	10/09/2002	WIDE-RANGE LOCAL BIAS GENERATOR FOR BODY BIAS GRID	TANG, STEPHEN H.
10330652	7200068	150	12/27/2002	MULTI-PORTED REGISTER FILES	TANG, STEPHEN H.
10334644	6710642	150	12/30/2002	BIAS GENERATION CIRCUIT	TANG, STEPHEN H.
10673283	Not Issued	161	09/30/2003	Local bias generator for adaptive forward body bias	TANG, STEPHEN H.
10689128	6975005	150	10/20/2003	CURRENT REFERENCE APPARATUS AND SYSTEMS	TANG, STEPHEN H.

10716755	7072205	150	11/19/2003	FLOATING-BODY DRAM WITH TWO-PHASE WRITE	TANG, STEPHEN H.
10721184	7002842	150	11/26/2003	FLOATING-BODY DYNAMIC RANDOM ACCESS MEMORY WITH PURGE LINE	TANG, STEPHEN H.
10738216	7020041	150	12/18/2003	METHOD AND APPARATUS TO CLAMP SRAM SUPPLY VOLTAGE	TANG, STEPHEN H.
10740551	6952376	150	12/22/2003	METHOD AND APPARATUS TO GENERATE A REFERENCE VALUE IN A MEMORY ARRAY	TANG, STEPHEN H.
10746148	6906973	150	12/24/2003	BITE-LINE DROOP REDUCTION	TANG, STEPHEN H.
10747084	6870418	150	12/30/2003	TEMPERATURE AND/OR PROCESS INDEPENDENT CURRENT GENERATION CIRCUIT	TANG, STEPHEN H.
10749734	7123500	150	12/30/2003	1P1N 2T GAIN CELL	TANG, STEPHEN H.
10750566	7001811	150	12/31/2003	METHOD FOR MAKING MEMORY CELL WITHOUT HALO IMPLANT	TANG, STEPHEN H.
10750572	6992339	150	12/31/2003	ASYMMETRIC MEMORY CELL	TANG, STEPHEN H.
10812894	Not Issued	71	03/31/2004	SRAM device having forward body bias control	TANG, STEPHEN H.
10879480	7098507	150	06/30/2004	FLOATING-BODY DYNAMIC RANDOM ACCESS MEMORY AND METHOD OF FABRICATION IN TRI-GATE TECHNOLOGY	TANG, STEPHEN H.
10879486	Not Issued	61	06/30/2004	Method, apparatus and system of adjusting one or more performance-related parameters of a processor	TANG, STEPHEN H.
10880337	7102358	150	06/29/2004	OVERVOLTAGE DETECTION APPARATUS, METHOD, AND SYSTEM	TANG, STEPHEN H.
10881001	7120072	150	06/30/2004	TWO TRANSISTOR GAIN CELL, METHOD, AND SYSTEM	TANG, STEPHEN H.
10942019	Not Issued	71	09/16/2004	Charge storage memory cell	TANG, STEPHEN H.
10953865	Not	161	09/30/2004	System and method for applying	TANG, STEPHEN

	Issued			within-die adaptive body bias	H.
10954537	7110278	150	09/29/2004	CROSSPOINT MEMORY ARRAY UTILIZING ONE TIME PROGRAMMABLE ANTIFUSE CELLS	TANG, STEPHEN H.
10954931	7061806	150	09/30/2004	FLOATING-BODY MEMORY CELL WRITE	TANG, STEPHEN H.
10956195	7206249	150	09/30/2004	SRAM CELL POWER REDUCTION CIRCUIT	TANG, STEPHEN H.
10956285	Not Issued	93	09/30/2004	NON VOLATILE DATA STORAGE THROUGH DIELECTRIC BREAKDOWN	TANG, STEPHEN H.
10956407	7075821	150	09/30/2004	APPARATUS AND METHOD FOR A ONE-PHASE WRITE TO A ONE-TRANSISTOR MEMORY CELL ARRAY	TANG, STEPHEN H.
10979605	7102951	150	11/01/2004	OTP ANTIFUSE CELL AND CELL ARRAY	TANG, STEPHEN H.
10982266	7106128	150	11/03/2004	PROCESSOR APPARATUS WITH BODY BIAS CIRCUITRY TO DELAY THERMAL THROTTLING	TANG, STEPHEN H.
11008666	Not Issued	90	02/22/2005	2-TRANSISTOR FLOATING-BODY DRAM	TANG, STEPHEN H.
11027476	Not Issued	61	12/28/2004	One time programmable memory	TANG, STEPHEN H.
11038134	7164307	150	01/21/2005	BIAS GENERATOR FOR BODY BIAS	TANG, STEPHEN H.
11038394	7236045	150	01/21/2005	BIAS GENERATOR FOR BODY BIAS	TANG, STEPHEN H.
11053786	Not Issued	161	02/09/2005	Non strobe sensing circuit	TANG, STEPHEN H.
11134450	Not Issued	95	05/23/2005	REDUCING POWER CONSUMPTION IN INTEGRATED CIRCUITS	TANG, STEPHEN H.
11151982	7230846	150	06/14/2005	PURGE-BASED FLOATING BODY MEMORY	TANG, STEPHEN H.
11158518	7167397	150	06/21/2005	APPARATUS AND METHOD FOR PROGRAMMING A MEMORY ARRAY	TANG, STEPHEN H.
11170504	7262107	150	06/29/2005	CAPACITOR STRUCTURE FOR A LOGIC PROCESS	TANG, STEPHEN H.
11239903	7280425	150	09/30/2005	DUAL GATE OXIDE ONE TIME PROGRAMMABLE (OTP)	TANG, STEPHEN H.

				ANTIFUSE CELL	
11268098	Not Issued	61	11/07/2005	Asymmetric memory cell	TANG, STEPHEN H.
11268430	Not Issued	41	11/07/2005	Memory cell without halo implant	TANG, STEPHEN H.
11289621	7057927	150	11/30/2005	FLOATING-BODY DYNAMIC RANDOM ACCESS MEMORY WITH PURGE LINE	TANG, STEPHEN H.
11295400	Not Issued	30	12/06/2005	Component reliability budgeting system	TANG, STEPHEN H.
11320789	Not Issued	93	12/30/2005	METHOD AND APPARATUS TO CLAMP SRAM SUPPLY VOLTAGE	TANG, STEPHEN H.

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Inventor Name Search Result

Your Search was:

Last Name = KHELLAH
First Name = MUHAMMAD

Application#	Patent#	Status	Date Filed	Title	Inventor Name
10117163	6724648	150	04/05/2002	SRAM ARRAY WITH DYNAMIC VOLTAGE FOR REDUCING ACTIVE LEAKAGE POWER	KHELLAH, MUHAMMAD
10748222	6903984	150	12/31/2003	FLOATING-BODY DRAM USING WRITE WORD LINE FOR INCREASED RETENTION TIME	KHELLAH, MUHAMMAD
10750566	7001811	150	12/31/2003	METHOD FOR MAKING MEMORY CELL WITHOUT HALO IMPLANT	KHELLAH, MUHAMMAD
11066395	7031203	150	02/28/2005	FLOATING-BODY DRAM USING WRITE WORD LINE FOR INCREASED RETENTION TIME	KHELLAH, MUHAMMAD
11648490	Not Issued	17	12/28/2006	Memory cell bit valve loss detection and restoration	KHELLAH, MUHAMMAD
10273627	6801463	150	10/17/2002	METHOD AND APPARATUS FOR LEAKAGE COMPENSATION WITH FULL VCC PRE-CHARGE	KHELLAH, MUHAMMAD M.
10305753	6909652	150	11/26/2002	SRAM BIT-LINE REDUCTION	KHELLAH, MUHAMMAD M.
10330652	7200068	150	12/27/2002	MULTI-PORTED REGISTER FILES	KHELLAH, MUHAMMAD M.
10334410	6784688	150	12/30/2002	SKEWED REPEATER BUS	KHELLAH, MUHAMMAD M.
10334456	6831871	150	12/30/2002	STABLE MEMORY CELL READ	KHELLAH, MUHAMMAD M.
10334746	Not Issued	71	12/31/2002	Method and apparatus for bus repeater tapering	KHELLAH, MUHAMMAD M.
10716755	7072205	150	11/19/2003	FLOATING-BODY DRAM WITH TWO-PHASE WRITE	KHELLAH, MUHAMMAD M.

10721184	7002842	150	11/26/2003	FLOATING-BODY DYNAMIC RANDOM ACCESS MEMORY WITH PURGE LINE	KHELLAH, MUHAMMAD M.
10738216	7020041	150	12/18/2003	METHOD AND APPARATUS TO CLAMP SRAM SUPPLY VOLTAGE	KHELLAH, MUHAMMAD M.
10738220	6876571	150	12/18/2003	STATIC RANDOM ACCESS MEMORY HAVING LEAKAGE REDUCTION CIRCUIT	KHELLAH, MUHAMMAD M.
10740551	6952376	150	12/22/2003	METHOD AND APPARATUS TO GENERATE A REFERENCE VALUE IN A MEMORY ARRAY	KHELLAH, MUHAMMAD M.
10746148	6906973	150	12/24/2003	BITE-LINE DROOP REDUCTION	KHELLAH, MUHAMMAD M.
10749734	7123500	150	12/30/2003	1P1N 2T GAIN CELL	KHELLAH, MUHAMMAD M.
10750572	6992339	150	12/31/2003	ASYMMETRIC MEMORY CELL	KHELLAH, MUHAMMAD M.
10810093	6985380	150	03/26/2004	SRAM WITH FORWARD BODY BIASING TO IMPROVE READ CELL STABILITY	KHELLAH, MUHAMMAD M.
10812894	Not Issued	71	03/31/2004	SRAM device having forward body bias control	KHELLAH, MUHAMMAD M.
10813084	6992603	150	03/31/2004	SINGLE-STAGE AND MULTI-STAGE LOW POWER INTERCONNECT ARCHITECTURES	KHELLAH, MUHAMMAD M.
10879480	7098507	150	06/30/2004	FLOATING-BODY DYNAMIC RANDOM ACCESS MEMORY AND METHOD OF FABRICATION IN TRI-GATE TECHNOLOGY	KHELLAH, MUHAMMAD M.
10880337	7102358	150	06/29/2004	OVERVOLTAGE DETECTION APPARATUS, METHOD, AND SYSTEM	KHELLAH, MUHAMMAD M.
10880988	Not Issued	93	06/30/2004	INTERCONNECT STRUCTURE IN INTEGRATED CIRCUITS	KHELLAH, MUHAMMAD M.
10881001	7120072	150	06/30/2004	TWO TRANSISTOR GAIN CELL, METHOD, AND SYSTEM	KHELLAH, MUHAMMAD M.
10942019	Not	71	09/16/2004	Charge storage memory cell	KHELLAH,

	Issued				MUHAMMAD M.
10947765	7183795	150	09/23/2004	MAJORITY VOTER APPARATUS, SYSTEMS, AND METHODS	KHELLAH, MUHAMMAD M.
10954537	7110278	150	09/29/2004	CROSSPOINT MEMORY ARRAY UTILIZING ONE TIME PROGRAMMABLE ANTIFUSE CELLS	KHELLAH, MUHAMMAD M.
10954931	7061806	150	09/30/2004	FLOATING-BODY MEMORY CELL WRITE	KHELLAH, MUHAMMAD M.
10956195	7206249	150	09/30/2004	SRAM CELL POWER REDUCTION CIRCUIT	KHELLAH, MUHAMMAD M.
10956285	Not Issued	93	09/30/2004	NON VOLATILE DATA STORAGE THROUGH DIELECTRIC BREAKDOWN	KHELLAH, MUHAMMAD M.
10956407	7075821	150	09/30/2004	APPARATUS AND METHOD FOR A ONE-PHASE WRITE TO A ONE-TRANSISTOR MEMORY CELL ARRAY	KHELLAH, MUHAMMAD M.
10979605	7102951	150	11/01/2004	OTP ANTIFUSE CELL AND CELL ARRAY	KHELLAH, MUHAMMAD M.
11001870	Not Issued	93	12/01/2004	MEMORY CIRCUIT	KHELLAH, MUHAMMAD M.
11008666	Not Issued	90	02/22/2005	2-TRANSISTOR FLOATING-BODY DRAM	KHELLAH, MUHAMMAD M.
11027476	Not Issued	61	12/28/2004	One time programmable memory	KHELLAH, MUHAMMAD M.
11053786	Not Issued	161	02/09/2005	Non strobe sensing circuit	KHELLAH, MUHAMMAD M.
11053788	7236005	150	02/09/2005	MAJORITY VOTER CIRCUIT DESIGN	KHELLAH, MUHAMMAD M.
11059174	Not Issued	41	02/16/2005	Representative majority voter for bus invert coding	KHELLAH, MUHAMMAD M.
11134450	Not Issued	95	05/23/2005	REDUCING POWER CONSUMPTION IN INTEGRATED CIRCUITS	KHELLAH, MUHAMMAD M.
11137905	Not Issued	161	05/25/2005	Memory with dynamically adjustable supply	KHELLAH, MUHAMMAD M.
11151982	7230846	150	06/14/2005	PURGE-BASED FLOATING BODY MEMORY	KHELLAH, MUHAMMAD M.
11158518	7167397	150	06/21/2005	APPARATUS AND METHOD FOR PROGRAMMING A MEMORY ARRAY	KHELLAH, MUHAMMAD M.
11169106	7236410	150	06/27/2005	MEMORY CELL DRIVER	KHELLAH,

				CIRCUITS	MUHAMMAD M.
11170504	7262107	150	06/29/2005	CAPACITOR STRUCTURE FOR A LOGIC PROCESS	KHELLAH, MUHAMMAD M.
11172078	Not Issued	161	06/29/2005	Memory circuit	KHELLAH, MUHAMMAD M.
11172742	7295474	150	06/30/2005	OPERATING AN INFORMATION STORAGE CELL ARRAY	KHELLAH, MUHAMMAD M.
11225912	7230842	150	09/13/2005	MEMORY CELL HAVING P-TYPE PASS DEVICE	KHELLAH, MUHAMMAD M.
11239903	7280425	150	09/30/2005	DUAL GATE OXIDE ONE TIME PROGRAMMABLE (OTP) ANTIFUSE CELL	KHELLAH, MUHAMMAD M.

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Inventor Name Search Result

Your Search was:

Last Name = SOMASEKHAR
First Name = DINESH

Application#	Patent#	Status	Date Filed	Title	Inventor Name
08412183	Not Issued	161	03/28/1995	APPARATUS AND METHOD FOR A REDUCED POWER MEMORY DIFFERENTIAL VOLTAGE SENSE-AMPLIFIER	SOMASEKHAR, DINESH
08937832	6014041	150	09/26/1997	DIFFERENTIAL CURRENT SWITCH LOGIC GATE	SOMASEKHAR, DINESH
08997071	6002272	150	12/23/1997	TRI-RAIL DOMINO CIRCUIT	SOMASEKHAR, DINESH
09539933	6421289	150	03/31/2000	METHOD AND APPARATUS FOR CHARGE-TRANSFER PRE-SENSING	SOMASEKHAR, DINESH
09690513	6496402	150	10/17/2000	NOISE SUPPRESSION FOR OPEN BIT LINE DRAM ARCHITECTURES	SOMASEKHAR, DINESH
09690687	6421269	150	10/17/2000	LOW-LEAKAGE MOS PLANAR CAPACITORS FOR USE WITHIN DRAM STORAGE CELLS	SOMASEKHAR, DINESH
09733216	6459316	150	12/08/2000	FLIP FLOP CIRCUIT	SOMASEKHAR, DINESH
09733482	6701339	150	12/08/2000	PIPELINED COMPRESSOR CIRCUIT	SOMASEKHAR, DINESH
09740104	6351156	150	12/18/2000	Noise reduction circuit	SOMASEKHAR, DINESH
09796072	6982589	150	02/28/2001	MULTI-STAGE MULTIPLEXER	SOMASEKHAR, DINESH
09823575	6608786	150	03/30/2001	APPARATUS AND METHOD FOR A MEMORY STORAGE CELL LEAKAGE CANCELLATION SCHEME	SOMASEKHAR, DINESH
09873557	7080111	150	06/04/2001	FLOATING POINT MULTIPLY ACCUMULATOR	SOMASEKHAR, DINESH

09873721	6889241	150	06/04/2001	FLOATING POINT ADDER	SOMASEKHAR, DINESH
09941053	6567329	150	08/28/2001	MULTIPLE WORD-LINE ACCESSING AND ACCESSOR	SOMASEKHAR, DINESH
09966586	6757784	150	09/28/2001	HIDING REFRESH OF MEMORY AND REFRESH-HIDDEN MEMORY	SOMASEKHAR, DINESH
10117163	6724648	150	04/05/2002	SRAM ARRAY WITH DYNAMIC VOLTAGE FOR REDUCING ACTIVE LEAKAGE POWER	SOMASEKHAR, DINESH
10208130	6597223	150	07/30/2002	FLIP FLOP CIRCUIT	SOMASEKHAR, DINESH
10241791	6707708	150	09/10/2002	STATIC RANDOM ACCESS MEMORY WITH SYMMETRIC LEAKAGE-COMPENSATED BIT LINE	SOMASEKHAR, DINESH
10267951	6784722	150	10/09/2002	WIDE-RANGE LOCAL BIAS GENERATOR FOR BODY BIAS GRID	SOMASEKHAR, DINESH
10273627	6801463	150	10/17/2002	METHOD AND APPARATUS FOR LEAKAGE COMPENSATION WITH FULL VCC PRE-CHARGE	SOMASEKHAR, DINESH
10300398	6721222	150	11/19/2002	NOISE SUPPRESSION FOR OPEN BIT LINE DRAM ARCHITECTURES	SOMASEKHAR, DINESH
10305753	6909652	150	11/26/2002	SRAM BIT-LINE REDUCTION	SOMASEKHAR, DINESH
10316728	6707755	150	12/11/2002	HIGH VOLTAGE DRIVER	SOMASEKHAR, DINESH
10324177	6879531	150	12/19/2002	REDUCED READ DELAY FOR SINGLE-ENDED SENSING	SOMASEKHAR, DINESH
10324178	6724649	150	12/19/2002	MEMORY CELL LEAKAGE REDUCTION	SOMASEKHAR, DINESH
10334456	6831871	150	12/30/2002	STABLE MEMORY CELL READ	SOMASEKHAR, DINESH
10461293	6801465	150	06/13/2003	APPARATUS AND METHOD FOR A MEMORY STORAGE CELL LEAKAGE CANCELLATION SCHEME	SOMASEKHAR, DINESH
10691342	Not	161	10/21/2003	Hiding refresh of memory and	SOMASEKHAR,

	Issued			refresh-hidden memory	DINESH
10716755	7072205	150	11/19/2003	FLOATING-BODY DRAM WITH TWO-PHASE WRITE	SOMASEKHAR, DINESH
10721178	7246215	150	11/26/2003	SYSTOLIC MEMORY ARRAYS	SOMASEKHAR, DINESH
10721184	7002842	150	11/26/2003	FLOATING-BODY DYNAMIC RANDOM ACCESS MEMORY WITH PURGE LINE	SOMASEKHAR, DINESH
10738216	7020041	150	12/18/2003	METHOD AND APPARATUS TO CLAMP SRAM SUPPLY VOLTAGE	SOMASEKHAR, DINESH
10738220	6876571	150	12/18/2003	STATIC RANDOM ACCESS MEMORY HAVING LEAKAGE REDUCTION CIRCUIT	SOMASEKHAR, DINESH
10740551	6952376	150	12/22/2003	METHOD AND APPARATUS TO GENERATE A REFERENCE VALUE IN A MEMORY ARRAY	SOMASEKHAR, DINESH
10746148	6906973	150	12/24/2003	BITE-LINE DROOP REDUCTION	SOMASEKHAR, DINESH
10748222	6903984	150	12/31/2003	FLOATING-BODY DRAM USING WRITE WORD LINE FOR INCREASED RETENTION TIME	SOMASEKHAR, DINESH
10749734	7123500	150	12/30/2003	1P1N 2T GAIN CELL	SOMASEKHAR, DINESH
10750566	7001811	150	12/31/2003	METHOD FOR MAKING MEMORY CELL WITHOUT HALO IMPLANT	SOMASEKHAR, DINESH
10750572	6992339	150	12/31/2003	ASYMMETRIC MEMORY CELL	SOMASEKHAR, DINESH
10810093	6985380	150	03/26/2004	SRAM WITH FORWARD BODY BIASING TO IMPROVE READ CELL STABILITY	SOMASEKHAR, DINESH
10812894	Not Issued	71	03/31/2004	SRAM device having forward body bias control	SOMASEKHAR, DINESH
10879480	7098507	150	06/30/2004	FLOATING-BODY DYNAMIC RANDOM ACCESS MEMORY AND METHOD OF FABRICATION IN TRI-GATE TECHNOLOGY	SOMASEKHAR, DINESH

10880337	7102358	150	06/29/2004	OVERVOLTAGE DETECTION APPARATUS, METHOD, AND SYSTEM	SOMASEKHAR, DINESH
10881001	7120072	150	06/30/2004	TWO TRANSISTOR GAIN CELL, METHOD, AND SYSTEM	SOMASEKHAR, DINESH
10942019	Not Issued	71	09/16/2004	Charge storage memory cell	SOMASEKHAR, DINESH
10947869	7109776	150	09/23/2004	GATING FOR DUAL EDGE-TRIGGERED CLOCKING	SOMASEKHAR, DINESH
10954537	7110278	150	09/29/2004	CROSSPOINT MEMORY ARRAY UTILIZING ONE TIME PROGRAMMABLE ANTIFUSE CELLS	SOMASEKHAR, DINESH
10954931	7061806	150	09/30/2004	FLOATING-BODY MEMORY CELL WRITE	SOMASEKHAR, DINESH
10956195	7206249	150	09/30/2004	SRAM CELL POWER REDUCTION CIRCUIT	SOMASEKHAR, DINESH
10956285	Not Issued	93	09/30/2004	NON VOLATILE DATA STORAGE THROUGH DIELECTRIC BREAKDOWN	SOMASEKHAR, DINESH

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Inventor Name Search Result

Your Search was:

Last Name = TSCHANZ
First Name = JAMES

Application#	Patent#	Status	Date Filed	Title	Inventor Name
10956195	7206249	150	09/30/2004	SRAM CELL POWER REDUCTION CIRCUIT	TSCHANZ, JAMES
11323675	Not Issued	71	12/30/2005	Error-detection flip-flop	TSCHANZ, JAMES
09608314	6429711	150	06/30/2000	STACK-BASED IMPULSE FLIP-FLOP WITH STACK NODE PRE-CHARGE AND STACK NODE PRE-DISCHARGE	TSCHANZ, JAMES W.
09672696	6632686	150	09/29/2000	SILICON ON INSULATOR DEVICE DESIGN HAVING IMPROVED FLOATING BODY EFFECT	TSCHANZ, JAMES W.
09707528	6744301	150	11/07/2000	SYSTEM USING BODY-BIASED SLEEP TRANSISTORS TO REDUCE LEAKAGE POWER WHILE MINIMIZING PERFORMANCE PENALITIES AND NOISE	TSCHANZ, JAMES W.
09820579	6608513	150	03/28/2001	FLIP-FLOP CIRCUIT HAVING DUAL-EDGE TRIGGERED PULSE GENERATOR	TSCHANZ, JAMES W.
09846514	Not Issued	161	04/30/2001	CMOS bus pulsing	TSCHANZ, JAMES W.
09846604	6515513	150	04/30/2001	REDUCING LEAKAGE CURRENTS IN INTEGRATED CIRCUITS	TSCHANZ, JAMES W.
09894465	6763484	150	06/28/2001	BODY BIAS USING SCAN CHAINS	TSCHANZ, JAMES W.
10010046	6642765	150	12/06/2001	TRANSMISSION-GATE BASED FLIP-FLOP	TSCHANZ, JAMES W.
10267951	6784722	150	10/09/2002	WIDE-RANGE LOCAL BIAS GENERATOR FOR BODY	TSCHANZ, JAMES W.

				BIAS GRID	
10328573	7120804	150	12/23/2002	METHOD AND APPARATUS FOR REDUCING POWER CONSUMPTION THROUGH DYNAMIC CONTROL OF SUPPLY VOLTAGE AND BODY BIAS INCLUDING MAINTAINING A SUBSTANTIALLY CONSTANT OPERATING FREQUENCY	TSCHANZ, JAMES W.
10330544	6806739	150	12/30/2002	TIME-BORROWING N-ONLY CLOCKED CYCLE LATCH	TSCHANZ, JAMES W.
10334410	6784688	150	12/30/2002	SKEWED REPEATER BUS	TSCHANZ, JAMES W.
10334746	Not Issued	71	12/31/2002	Method and apparatus for bus repeater tapering	TSCHANZ, JAMES W.
10673283	Not Issued	161	09/30/2003	Local bias generator for adaptive forward body bias	TSCHANZ, JAMES W.
10703562	7096433	150	11/10/2003	METHOD FOR POWER CONSUMPTION REDUCTION	TSCHANZ, JAMES W.
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